#15 amdt e (MF) KA 3/7/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(RA-133, formerly RD-036)

In the Application of: SIDIROPOULOS et al.

Serial No: 09/372,879

Filed: August 12, 1999

Title: Integrated Circuit Having I/O Structures with Reduced Input Loss

Group Art Unit: 2814

Examiner: Farahani, D.

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office, Fax No. (703) 872-9317 on 03/03/03 Date

Adrienne Mullany (name of person signing this certificate)

Adrienne Mullany 03/03/03 Signature

FAX RECEIVED

MAR 3 2003

TECHNOLOGY CENTER 2800

Assistant Commissioner for Patents
Washington, DC 20231

Final Office Action Response

RESPONSE TO THE OFFICE ACTION DATED January 2, 2003

This is a response to the Final Office Action dated January 2, 2003. This Response seeks to place this application in condition for allowance. The Examiner's rejections have been addressed below. Claims 1-24 and 26-37 are pending and a copy of these claims are attached hereto as Appendix A. No new matter has been added.

Office Action

In the Office Action dated January 2, 2003 (hereinafter, "OFFICE ACTION"), claims 1-11, under 35 U.S.C. §102(e) were rejected as being anticipated by U.S. Patent No. 6,329,694 to Lee et al. (hereinafter, "Lee"). Furthermore, claims 12-22 were rejected under 35 U.S.C. §103(a) as being "unpatentable" over Lee and claims 23, 24, 26, 27 and 29-37 were rejected under 35 U.S.C. §103(a) as being "unpatentable" over Lee in view of a Japanese patent to Sakai et al. (hereinafter, "Sakai"). Finally, claim 28 was rejected under 35 U.S.C. §103(a) as "being unpatentable over Lee as applied to claim 23... and further in view of Microelectronic Circuits